What is claimed is:

1. A multibit storage cell, comprising:

a semiconductor substrate having source and drain regions separated by a channel region;

a charge storage layer on said substrate and including an insulator material incorporating embedded metal nanocrystals;

a gate electrode on said charge storage layer; and

bias voltages connected to said source and drain regions to produce asymmetric charging of said nanocrystals.

2. The storage cell of Claim 1, wherein said embedded nanocrystals include a first portion forming a first node located in the region of a source side junction with said channel and a second portion forming a second node located in the region of a drain side junction with said channel, said first and second nodes forming first and second storage elements.

3. The storage cell of Claim 1, wherein said insulator material includes a control layer between said gate electrode and said nanocrystals and a tunnel layer between said nanosrystals and said substrate.

4. The storage cell of Claim 1, wherein said gate electrode overlies said nanocrystals and said channel.

5. The storage cell of Claim 1, wherein said bias voltages are connected to write and to read multiple bits of data in said nanocrystals.

6. The storage cell of Claim 5, wherein said bias voltages include write voltages selected to independently write data to said first and second storage elements.

7. The storage cell of Claim 5, wherein said bias voltages include read voltages selected to independently read data from said first and second storage elements.

8. The storage cell of Claim 5, wherein said bias voltages include first and second write voltages connectable to said source and drain to write information to a first storage element, and being reversible to write information to a second storage element.

9. The storage cell of Claim 7, wherein said bias voltages further include first and second read voltages connectable to said source and drain to read information written to said first storage element, and reversible to read information written to said second storage element.

10. A method of producing a cell, having multibit storage, comprising:

forming on a semiconductor surface a thin layer of tunnel oxide;

depositing on said tunnel oxide a metal wetting film;

annealing the film to produce self-assembled nanocrystals on said tunnel oxide;

depositing a control oxide layer on said nanocrystals;

forming a control gate on said control oxide layer;

implanting said semiconductor surface to form self-aligned source and drain regions; and

supplying reversible source-to-drain bias voltages for asymmetrically charging first and second portion of said nanocyrstals near said source and drain regions, respectively.

11. The method of Claim 10, wherein supplying said bias voltages includes supplying first and second write bias voltages to said source and drain for writing information to said first portion of said nanocrystals and reversing said first and second write bias voltages for writing information to said second portion of said nanocyrstals.

12. The method of Claim 10, wherein supplying said bias voltages further includes supplying first and second read bias voltages to said source and drain for reading information written to said first portion of said nanocrystals and reversing said first and second read bias voltages for reading information written to said second portion of said nanocrystals.